In this embodiment, because the amount or width of the pixel electrode 28 overlapping the storage electrode part 42B of the drain electrode pattern 42 is reduced from 15 to 20μm in the prior art to 2 to 4μm, a potential short between the upper and lower pixel electrodes 28 can be prevented. Also, the drain electrode pattern 42 and the data line 26 are formed from the same layer with a uniform interval therebetween to uniformly maintain a parasitic capacitor Cds between the drain electrode 26 and the drain electrode pattern 42. Therefore, a deterioration of the data signal caused by a non-uniformity of the parasitic capacitor Cds is prevented.

The thin film transistor substrate of Fig. 3 is formed by the same method as described with respect to Fig. 2, except that the protective film is patterned to form the contact holes 44 and the pixel electrodes 28 are formed to have the shape shown in Fig. 3.

Referring to Fig. 4, there is shown an electrode arrangement of a thin film transistor substrate in a liquid crystal display according to a third embodiment of the present invention. When compared with the thin film transistor shown in Fig. 3, the thin film transistor substrate of Fig. 4 has the same constructional elements except that a drain electrode pattern 46 is formed to have an annular shape along the periphery of the pixel electrode 28. In this case, the drain electrode pattern 46 is formed in an annular shape and overlaps with the bottom periphery of the pixel electrode 28; unlike the U-shaped drain electrode patterns 36 and 42 in Fig. 2 and Fig. 3, respectively.

The drain electrode pattern 46 prevents light from leaking between the pixel electrode 28 and the gate line 24. The drain electrode pattern 46 is connected, via a contact hole 48 formed in a protective film on the drain electrode part 46A, to the pixel electrode 28. Accordingly, the contact hole for connecting the storage electrode part 46B to the